

Appl. No. 10/605,499
Amdt. dated January 24, 2006
Reply to Office action of November 02, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

5 Listing of Claims:

1. (Currently amended) A method of fabricating a liquid crystal -display device-, the method comprising the steps of:

providing a substrate;

forming a polysilicon layer over the substrate;

10 performing a first ~~photo-etching process~~ photo-etching process to define at least one active area and a bottom storage electrode over the substrate;

performing a second ~~photo-etching process~~ photo-etching process to form a first mask over the substrate;

15 performing a P-type ion implantation process by utilizing the first mask as a mask to form a source electrode and a drain electrode in the active area and to dope dopants into the bottom storage electrode simultaneously;

removing the first mask;

forming a metal layer over the substrate to cover the active area and the bottom storage electrode;

20 performing a third ~~photo-etching process~~ photo-etching process to form a gate electrode over the active area and to form a top storage electrode on the bottom storage electrode;

forming a first isolation layer over the substrate to cover the gate electrode and the top storage electrode;

25 performing a fourth ~~photo-etching process~~ photo-etching process to form at least one first contact hole electrically connected to the source electrode, the drain electrode, and the gate electrode;

forming a conductive layer over the first isolation layer to fill in the first contact

Appl. No. 10/605,499
Amdt. dated January 24, 2006
Reply to Office action of November 02, 2005

hole;

performing a fifth ~~photo-etching process~~ photo-etching process to form a source wire and a drain wire on the first isolation layer, the source wire and the drain wire being electrically connected to the source electrode and the drain electrode through the first contact hole respectively; and
forming a second isolation layer over the substrate to cover the first isolation layer, the source wire, and the drain wire.

2. (Original) The method of claim 1 wherein the substrate comprises a glass substrate or a quartz substrate.

3. (Original) The method of claim 1 wherein the method for forming the polysilicon layer further comprises the following steps:
performing a sputtering process to form an amorphous silicon layer on the surface of the substrate; and
performing an annealing process to re-crystallize the amorphous silicon layer to the polysilicon layer.

4. (Original) The method of claim 3 wherein the annealing process is an excimer laser annealing process.

5. (Original) The method of claim 1 wherein the P-type ion implantation process is a high concentration P-type ion implantation process to form the source electrode and the drain electrode.

6. (Currently amended) The method of claim 1 wherein a step for forming a third isolation layer over the entire substrate is performed before the second ~~photo-etching process~~ photo-etching process to cover the active area and the

Appl. No. 10/605,499

Amdt. dated January 24, 2006

Reply to Office action of November 02, 2005

bottom storage electrode.

7. (Current amended) The method of claim 6 wherein the material composition of the third isolation layer comprises ~~silicon oxide formed by utilizing tetra-ethyl-ortho-silicate (TEOS) as a reaction gas, silicon oxide, or silicon nitride~~
5 silicon oxide, silicon nitride, or silicon oxide which is formed by utilizing tetra-ethyl-ortho-silicate as a reaction gas.

8. (Original) The method of claim 1 wherein a step for forming a fourth isolation layer on
10 the entire substrate is performed after removing the first mask to cover the active area and the bottom storage electrode.

9. (Currently amended) The method of claim 8 wherein the material composition of the fourth isolation layer comprises ~~silicon oxide formed by utilizing tetra-ethyl-ortho-silicate (TEOS) as a reaction gas, silicon oxide, or silicon nitride~~
15 silicon oxide, silicon nitride, or silicon oxide which is formed by utilizing tetra-ethyl-ortho-silicate as a reaction gas.

10. (Original) The method of claim 1 wherein the material composition of the metal layer
20 comprises tungsten (W) or chrome (Cr).

11. (Original) The method of claim 1 wherein the first isolation layer comprises a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

25 12. (Original) The method of claim 1 wherein the source wire is used as a data line.

13. (Currently amended) The method of claim 1 wherein the second isolation layer is a planarization layer, and the second isolation layer comprises -a silicon- oxide layer, a

Appl. No. 10/605,499
Amdt. dated January 24, 2006
Reply to Office action of November 02, 2005

silicon nitride layer, or a silicon oxide layer formed by utilizing tetra-ethyl-ortho-silicate as a reaction gas.

14. (Original) The method of claim 1 wherein the material composition of the transparent
5 conductive layer comprises indium tin oxide (ITO) or indium zinc oxide (IZO).

15. (Currently amended) The method of claim 1 further comprising the following steps:
performing a sixth ~~photo-etching-process~~ photo-etching process to remove portions
of the second isolation layer to form at least one second contact hole electrically
10 connected to the drain wire;
forming a transparent conductive layer on the second isolation layer; and
performing a seventh ~~photo-etching-process~~ photo-etching process to remove
portions of the transparent conductive layer to form at least one pixel electrode on
the second isolation layer, each pixel electrode being electrically connected to
15 each drain wire through each second contact hole filled with the transparent
conductive layer.